Valleytronic Information Processing and Applications

Steven A. Vitale

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LINCOLN LABORATORY
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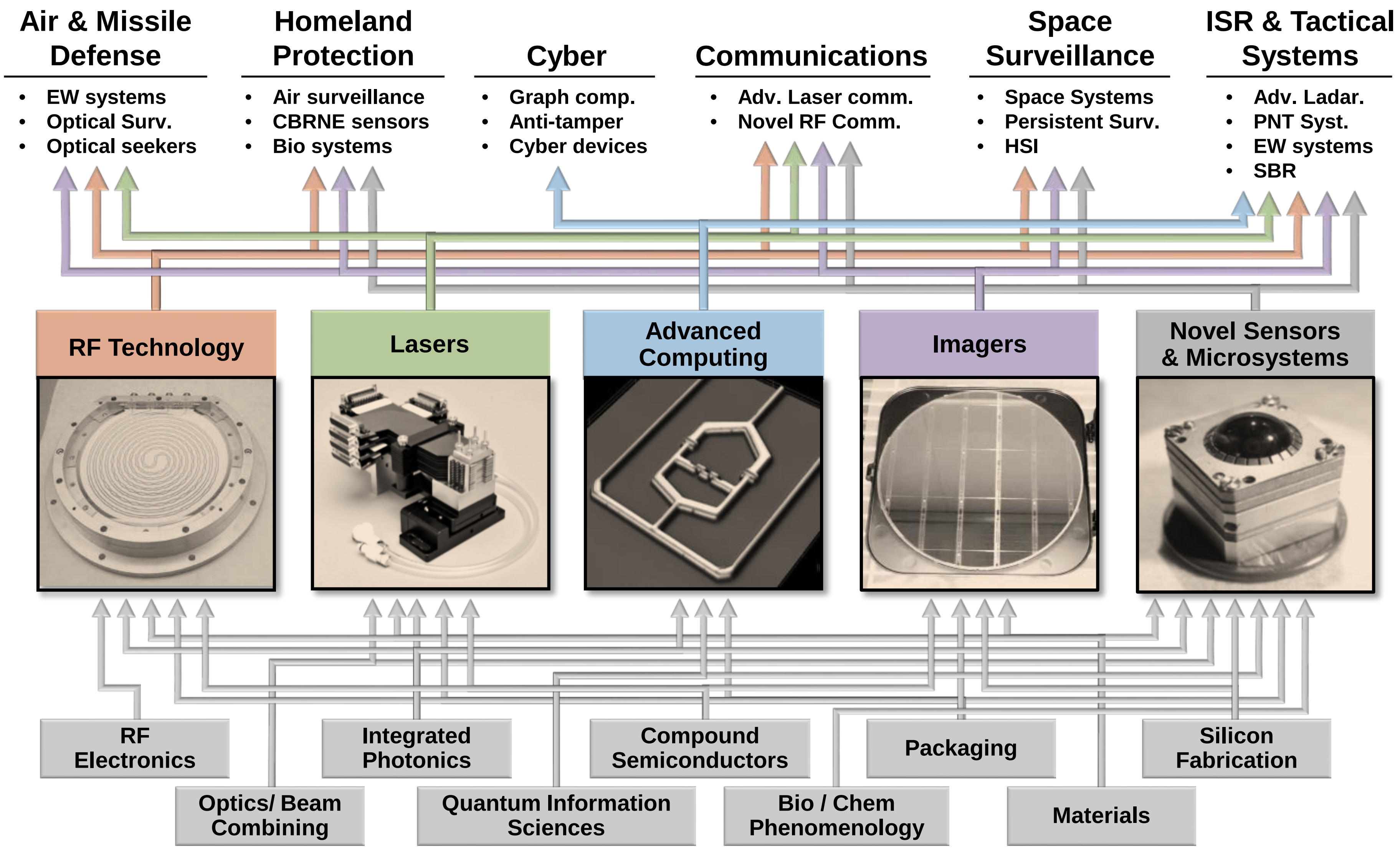
Advanced Technology Development



Materials That Made an Impact

Stone
2,600,000 years ago

Useful qualities: hard, durable, sharp

Applications: pounding, cutting, scraping

Wood
500,000 years ago

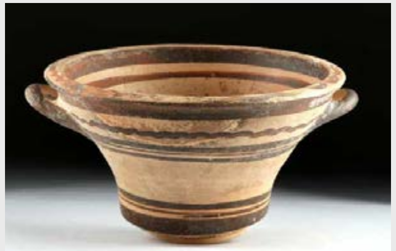
Useful qualities: light, easier to carve, ubiquitous

Applications: fuel, spears, handles, buildings, boats

Ceramics
20,000 years ago

Useful qualities: moldable, durable, easy to make, cheap as dirt

Applications: food storage, cooking



Metal Alloys
5,500 years ago

Strong, sharp, reusable, corrosion resistant

Applications: Swords, axes, arrowheads, plows, machinery

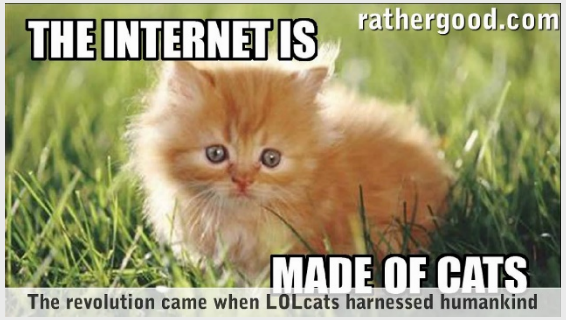
More Recently

Conductors
Polymers
Semiconductors
Dielectrics

150-200 Years Ago

Useful qualities: Transport and control of electrons

Applications: microelectronics



So, What’s Next?

Quantum Materials?
(Topological Insulators, Graphene, 2D TMDs, etc.)

A Few Years Ago

Useful qualities: ??

Applications: ???

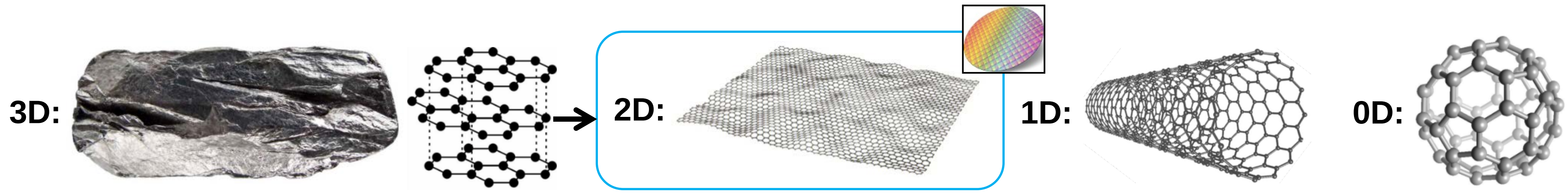
Potential Applications of Quantum Materials

Recently discovered physics phenomena in low dimensional materials may enable transformational performance or power advantages in electronic and photonic information processing systems

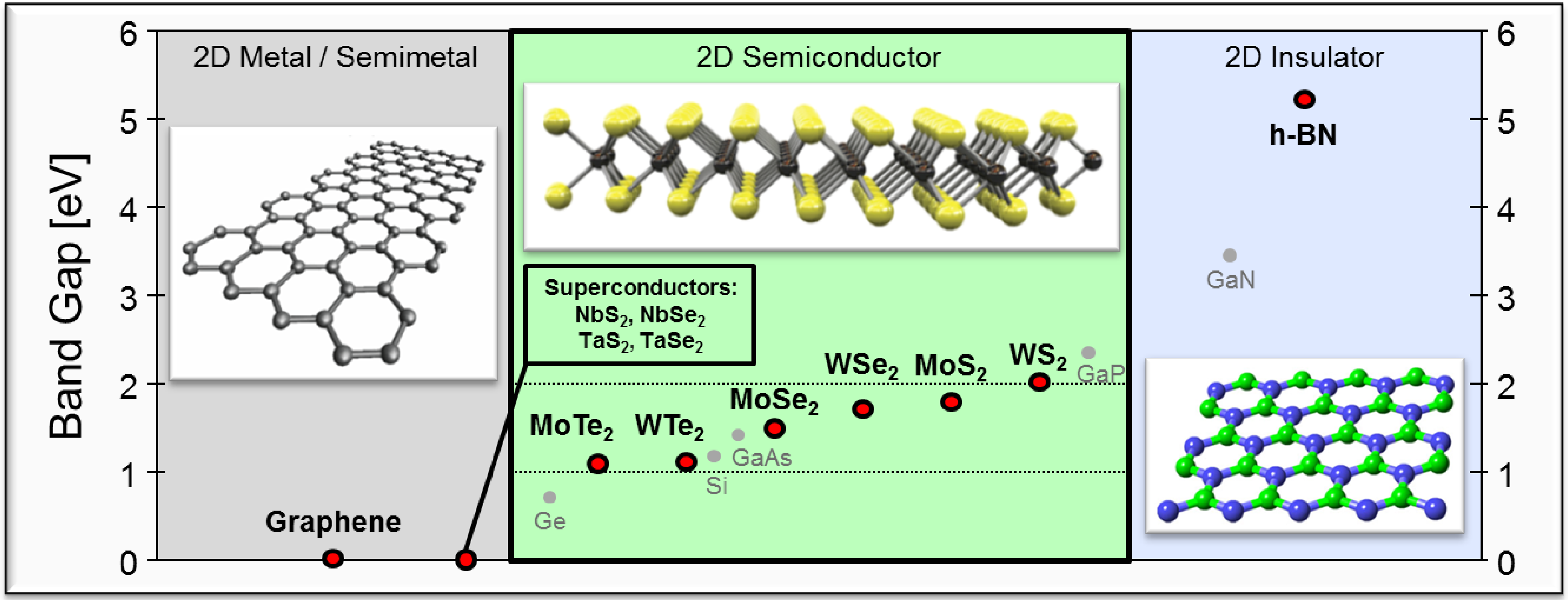
- **Beyond Moore's Law Computing: A new device for classical computing which is not constrained by the ubiquitous 60 mV/decade thermodynamic limit**
- **Quantum Computing: New qubit modalities with robust retain gate fidelity due to spin-valley locking**
- **Photonics: New integrated microphotonic non-reciprocal elements such as optical isolators**
- **Lasers: New energy-efficient, low-threshold on-chip lasers based on exciton polaritons**

Today's Focus

Two Dimensional Materials for Electronics



A Full Suite of Electronic Properties in 2D Materials



Monolayer Transition Metal Dichalcogenides

NANO LETTERS
pubs.acs.org/NanoLett

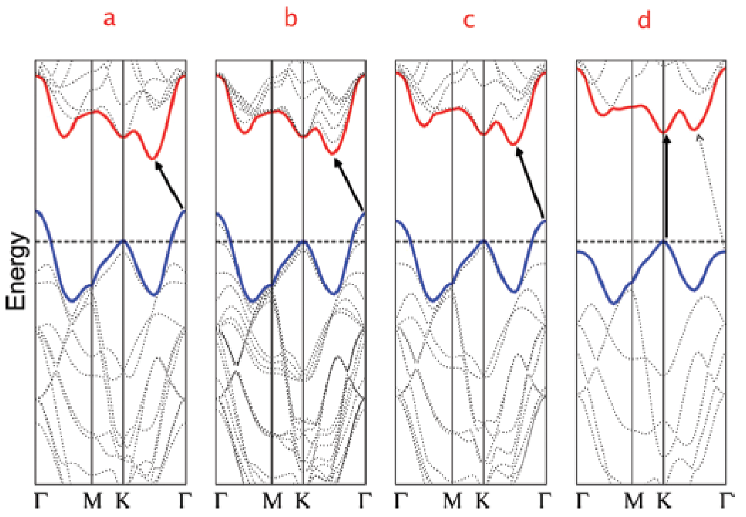
Emerging Photoluminescence in Monolayer MoS_2

Andrea Splendiani,[†,‡] Liang Sun,[†] Yuanbo Zhang,[†] Tianshu Li,[§] Jonghwan Kim,[†] Chi-Yung Chim,[†] Giulia Galli,[§] and Feng Wang*[,†,∥]

[†]Physics Department, University of California at Berkeley, Berkeley, California 94720, [‡]Scuola Galileiana di Studi Superiori di Padova, 35122 Padova, Italy, [§]Chemistry Department, University of California at Davis, Davis, California 95616, and [∥]Materials Science Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720

ABSTRACT Novel physical phenomena can emerge in low-dimensional nanomaterials. Bulk MoS_2, a prototypical metal dichalcogenide, is an indirect bandgap semiconductor with negligible photoluminescence. When the MoS_2 crystal is thinned to monolayer, however, a strong photoluminescence emerges, indicating an indirect to direct bandgap transition in this d-electron system. This observation shows that quantum confinement in layered d-electron materials like MoS_2 provides new opportunities for engineering the electronic structure of matter at the nanoscale.

KEYWORDS Photoluminescence, two-dimensional materials, metal dichalcogenide



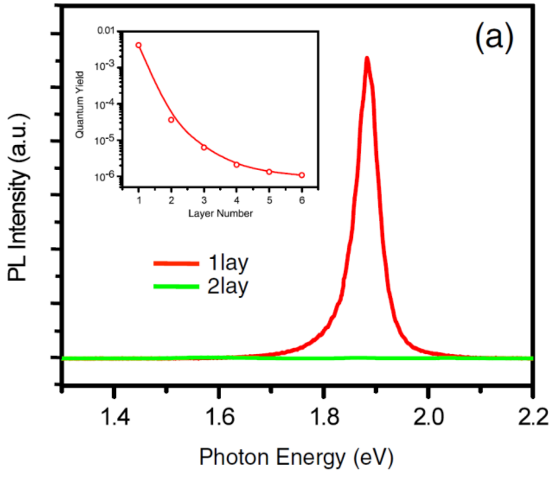
PRL 105, 136805 (2010) PHYSICAL REVIEW LETTERS week ending 24 SEPTEMBER 2010

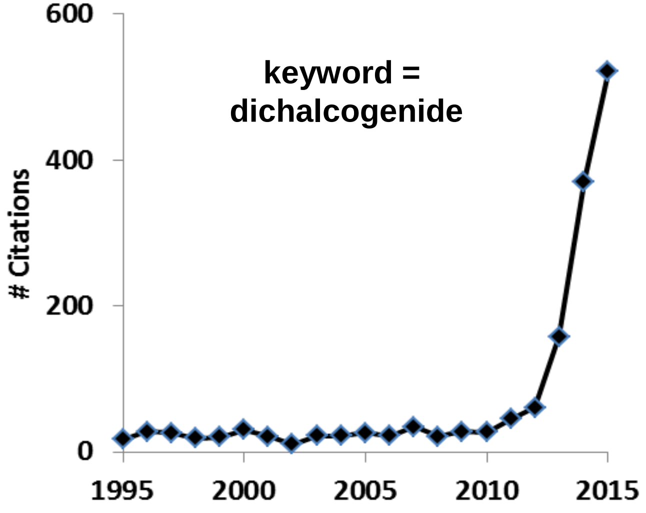
Atomically Thin MoS_2: A New Direct-Gap Semiconductor

Kin Fai Mak,[1] Changgu Lee,[2] James Hone,[3] Jie Shan,[4] and Tony F. Heinz[1,*]

[1]*Departments of Physics and Electrical Engineering, Columbia University, 538 West 120th Street, New York, New York 10027, USA*
[2]*SKKU Advanced Institute of Nanotechnology (SAINT) and Department of Mechanical Engineering, Sungkyunkwan University, Suwon 440-746, Korea*
[3]*Department of Mechanical Engineering, Columbia University, New York, New York 10027, USA*
[4]*Department of Physics, Case Western Reserve University, 10900 Euclid Avenue, Cleveland, Ohio 44106, USA*
(Received 2 April 2010; published 24 September 2010)

The electronic properties of ultrathin crystals of molybdenum disulfide consisting of $N = 1, 2, \ldots, 6$ S-Mo-S monolayers have been investigated by optical spectroscopy. Through characterization by absorption, photoluminescence, and photoconductivity spectroscopy, we trace the effect of quantum confinement on the material's electronic structure. With decreasing thickness, the indirect band gap, which lies below the direct gap in the bulk material, shifts upwards in energy by more than 0.6 eV. This leads to a crossover to a direct-gap material in the limit of the single monolayer. Unlike the bulk material, the MoS_2 monolayer emits light strongly. The freestanding monolayer exhibits an increase in luminescence quantum efficiency by more than a factor of 10^4 compared with the bulk material.

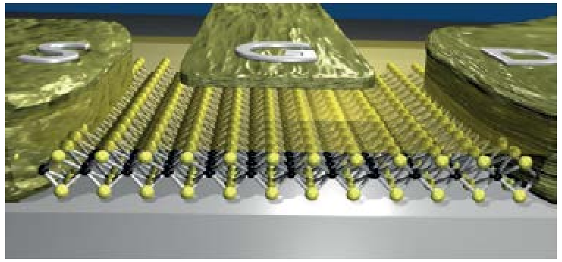




2D TMDs are unquestionably scientifically interesting. Can they be applied to solve our computational technology problem?

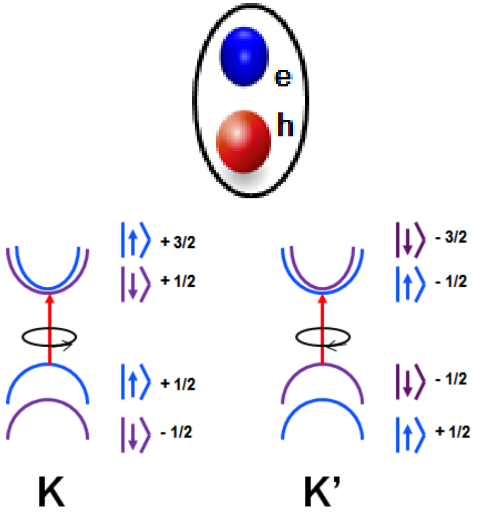
2D Transition Metal Dichalcogenide Properties

- Thin
  - Single monolayer < 10 Ǻ
- Stretchable
  - Strain up to 11% demonstrated
- Direct bandgap
- No surface states
  - No trap-induced device degradation
- Strong exciton binding energy
  - 200-500 meV vs 10's meV in bulk semiconductors
- Broken inversion symmetry
  - Valley contrasting Berry curvature & orbital magnetic moment
- Strong spin-orbit coupling



Fiori et al, 2014

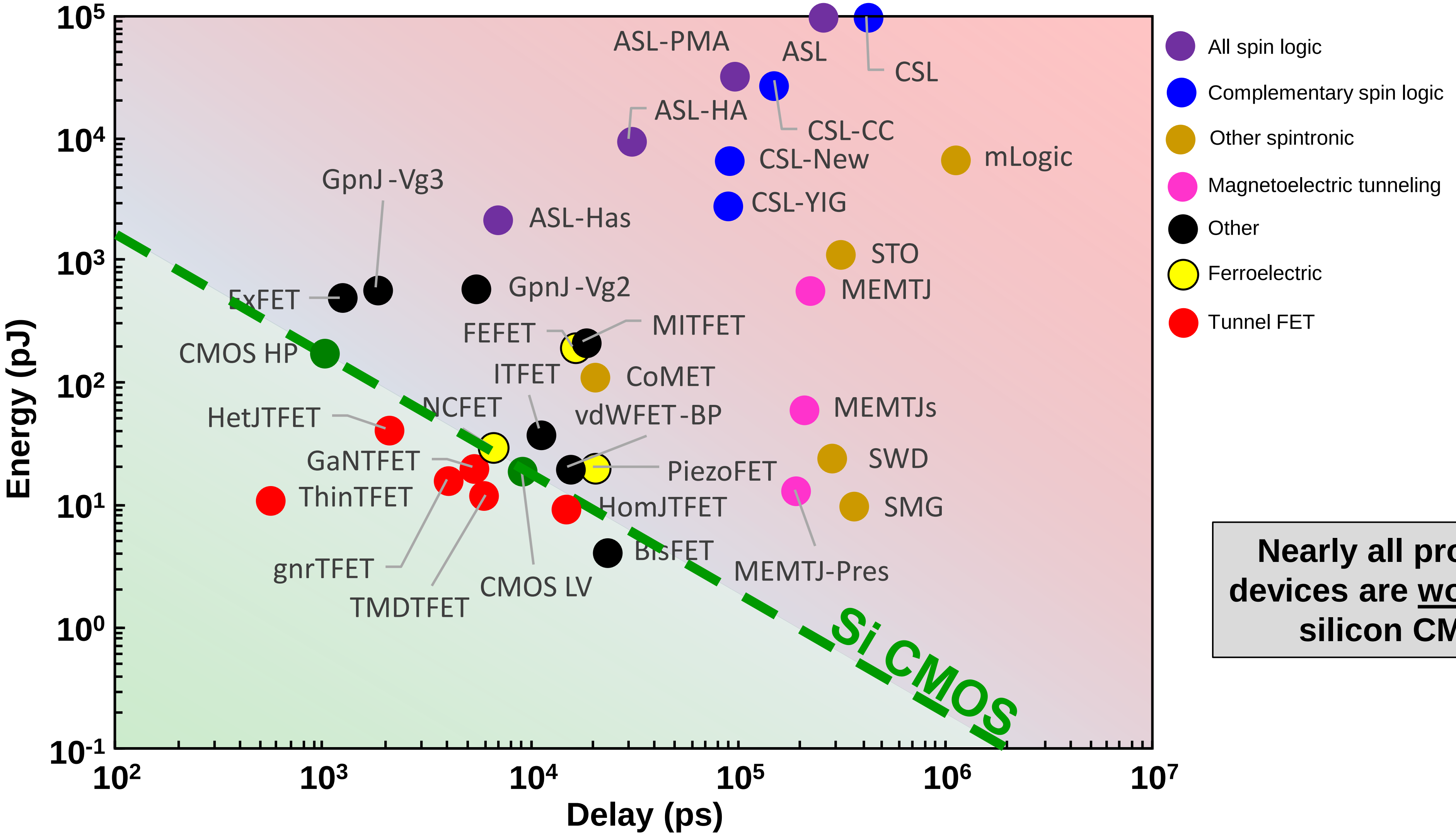
Flexible, transparent electronic/photonic devices



Can we exploit these properties to develop a logic device that outperforms silicon?

Zoology of Logic Devices to Outperform Silicon

Simulated Circuit Performance of Proposed Devices

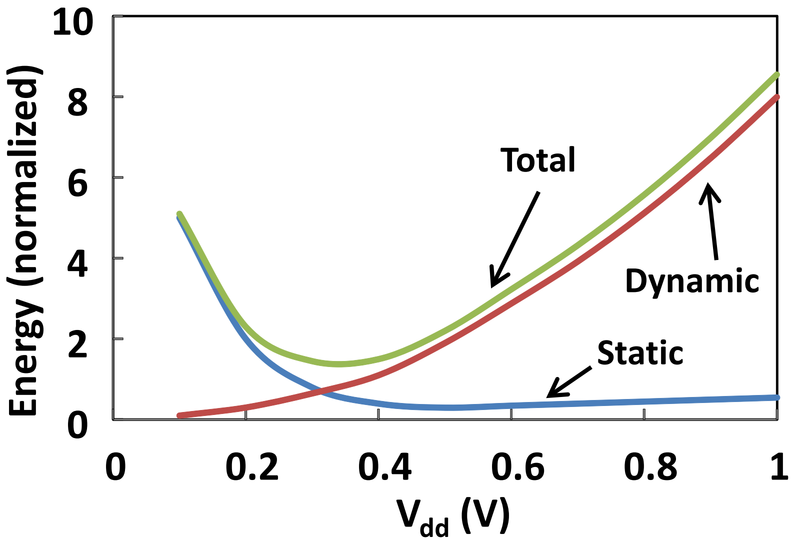


Nearly all proposed devices are worse than silicon CMOS!

32 bit ALU Simulations from Nikonov and Young, IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2015.

What's the fundamental problem here?

- Computation rate is limited by power, either available system power (e.g., cell phones) or dissipated power causing overheating (e.g., servers)
- Total power is the sum of static and dynamic (switching) power



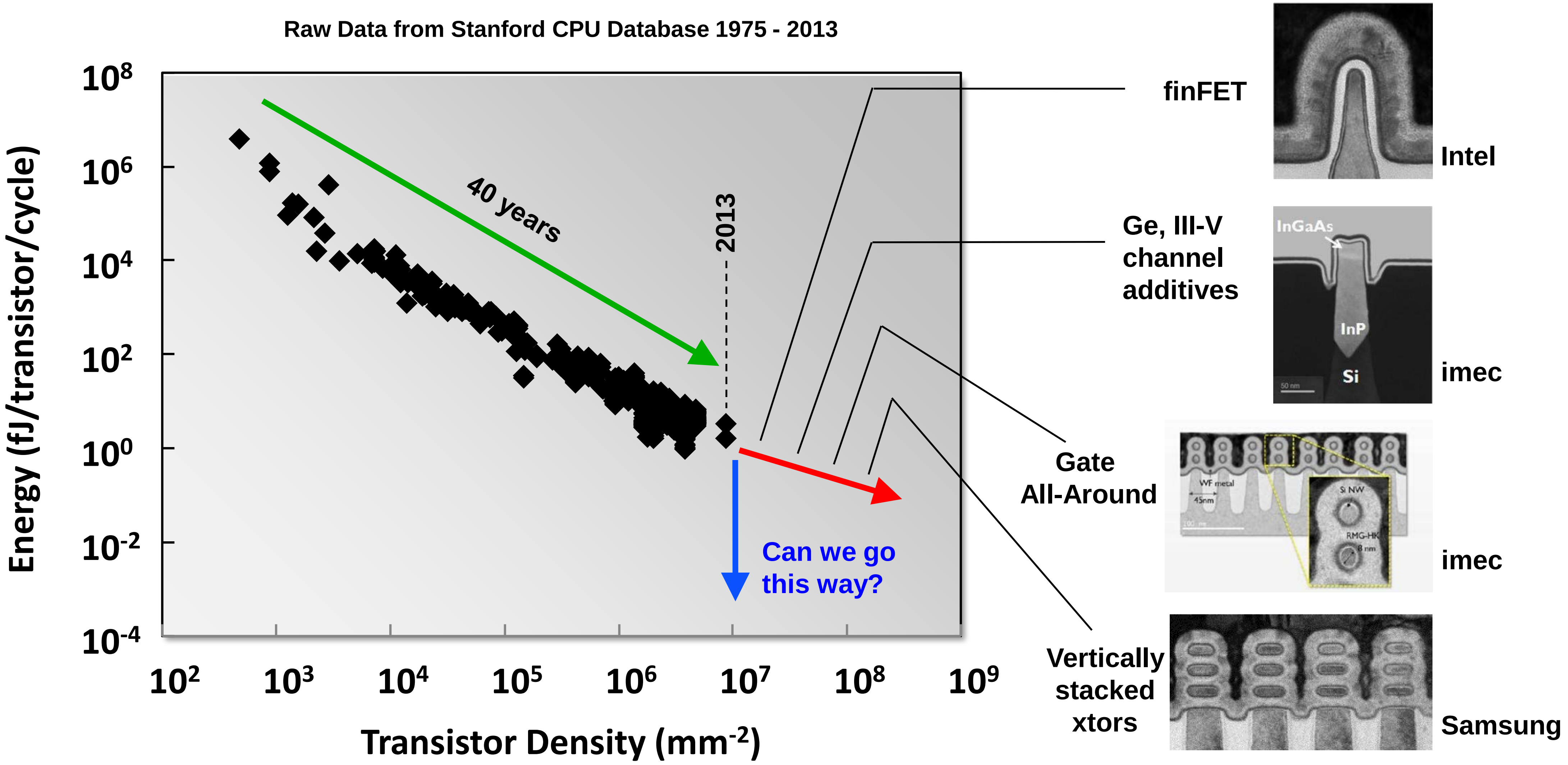
$$E_{dynamic} = \alpha C V^2$$

$$E_{static} = V_{dd} K e^{\left(\frac{V_g - V_t}{V_T}\right)} \left[1 - e^{-\frac{V_d}{V_T}}\right] \tau$$

- One way to reduce power is to make the device smaller

From Wang, VLSI, 2002

Switching Energy Near the End of Scaling



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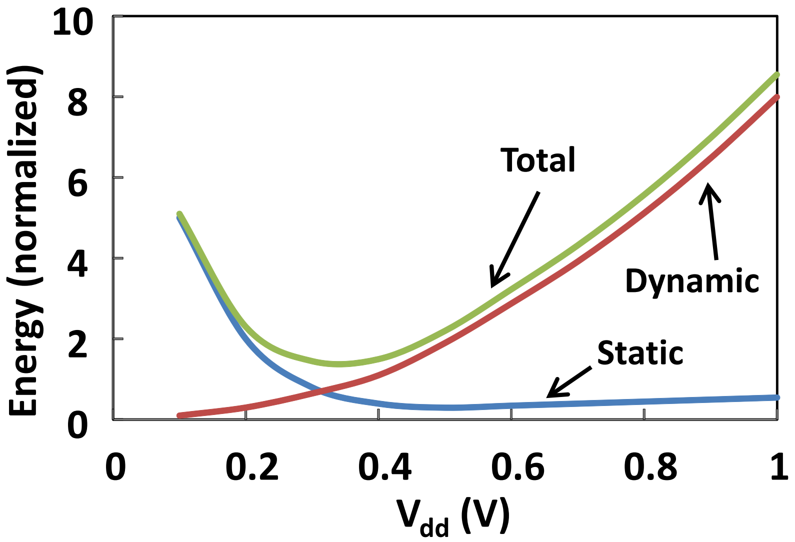

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$$E_{static} = V_{dd} K e^{\left(\frac{V_g - V_t}{V_T}\right)} \left[1 - e^{-\frac{V_d}{V_T}}\right] \tau$$

- One way to reduce power is to make the device smaller
- The most efficient way to reduce power is to reduce operating voltage

From Wang, VLSI, 2002

Thermodynamic Tyranny

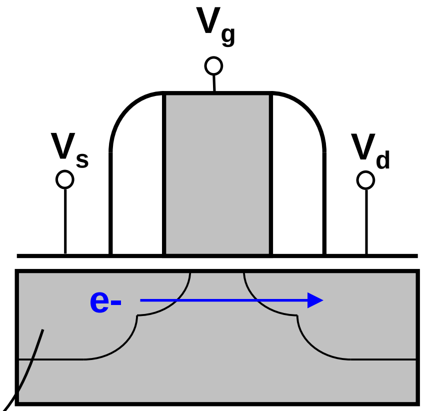
- Any switching device based on gated drift/diffusion of electrons will be limited to no more than one decade of current rise per 60 mV of V_{gs} at room temperature

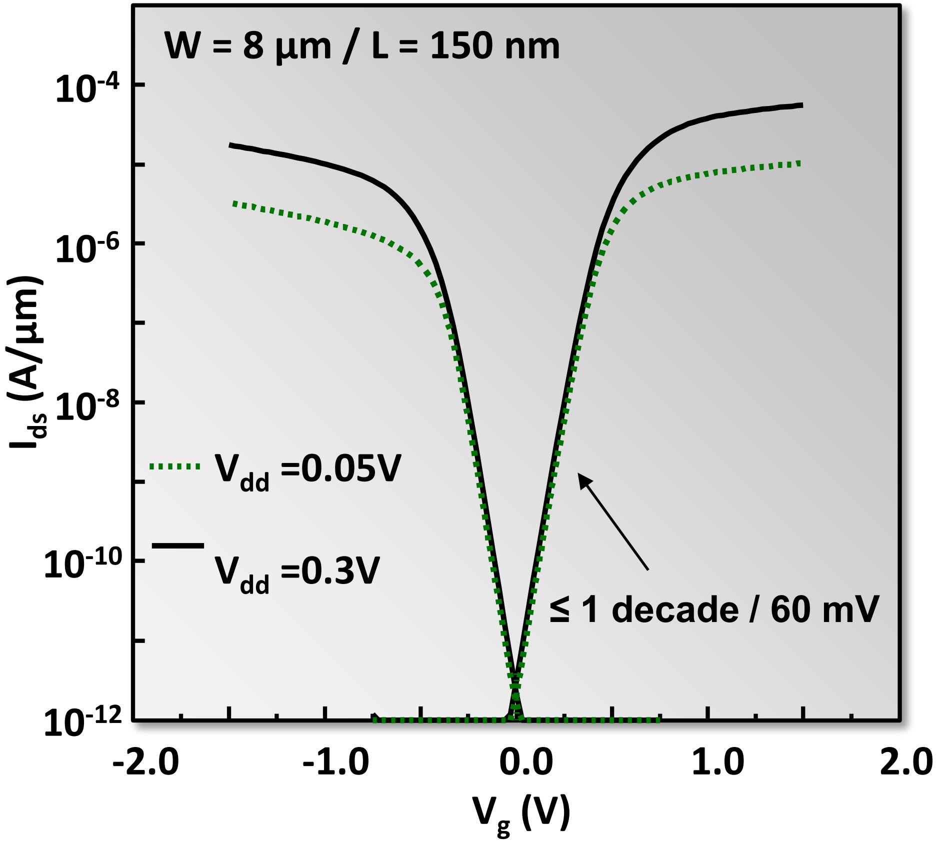
Long channel transistors

$$S = ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right)$$

$$f(E) = \frac{1}{1 + e^{(E-E_f)/kT}}$$

Fermi Dirac electron distribution





Taking into account static power, V_t variation, and stochastics across o(10^9) transistors, the minimum practical V_{DD} for high performance computing is ~ 0.6 V

Thermodynamic Tyranny

- Any switching device based on gated drift/diffusion of electrons will be limited to no more than one decade of current rise per 60 mV of V_{gs} at room temperature

What other options do we have for logic devices?

SpinFETs?	Well spin is usually carried by electrons, so …
TunnelFETs?	Possibly. Different set of challenges.
Photons?	Maybe, but would need $\lambda \approx$ 20nm to achieve competitive device size/speed

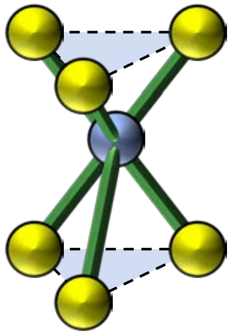
Are we done?

How about valleys?

Valleytronics Refresher

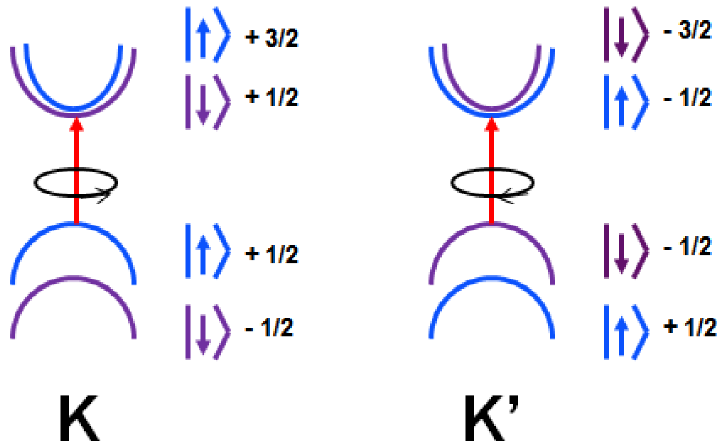
Valleytronics: Exploiting the crystal momentum state of real or quasi particles in 2D materials for something useful

2D Transition Metal Dichalcogenide



Material Properties

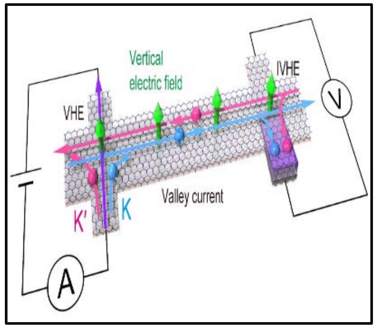
- Lack of inversion symmetry
- Time reversal symmetry
- Direct bandgap
- Strong spin orbit coupling



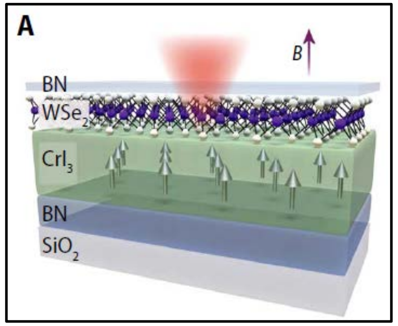
Two well-defined and accessible crystal momentum states, protected by spin-valley coupling

Interesting Properties

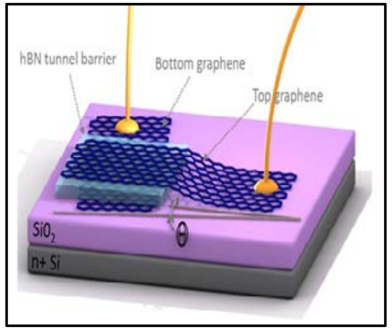
- Deterministic valley initialization
- Valley coupling to external fields
- Valley-specific state readout



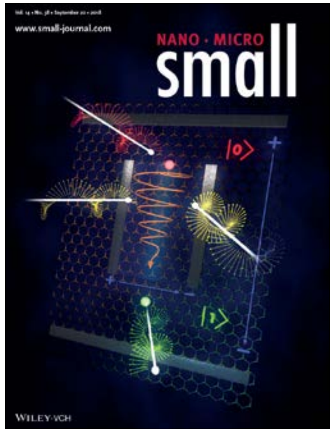
Valley Polarized Current Transport
[Shimazaki, Nature Physics, 2015]



Spin/valley injector
[Zhong, Sci Adv, 2017]



Moire potential
[Mischenko, Nature Nanotech, 2014]



[Vitale, Small, 2018]

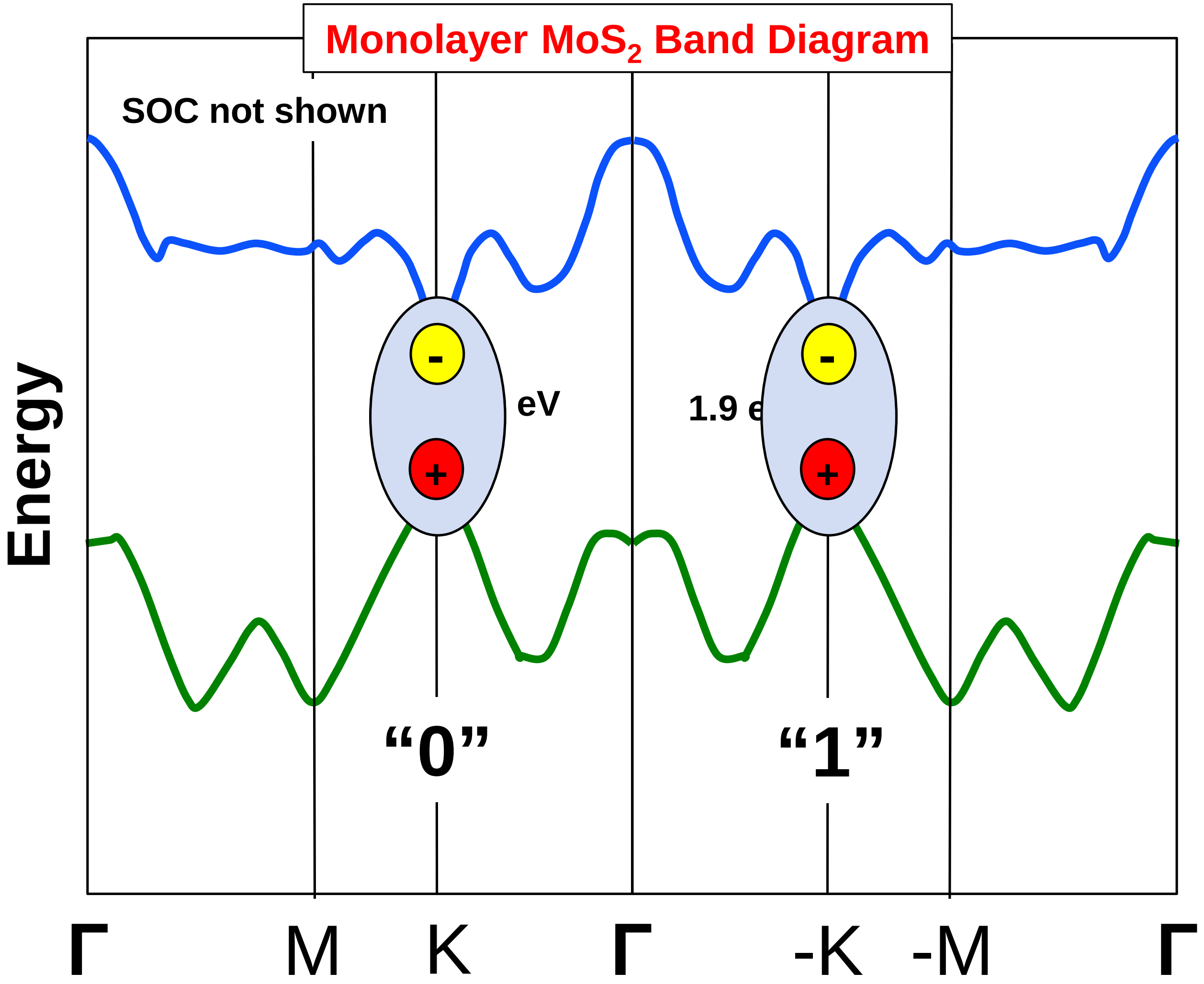
Let’s Look at the Valley Information Carrier Candidates

Information Carrier	Valley polarized	Spin polarized	Existing logic implementations	Low switching energy
Free electron	**Yes**	Slightly	**Yes**	Maybe
Free hole	**Yes**	Yes	**Yes**	Maybe
Exciton	**Yes**	No	**Not yet**	Maybe
Trion	Maybe	Maybe	**Not yet**	Maybe
Biexcitons, dark excitons etc.	**Inefficient generation and readout**			

Fermi function for valley-polarized e/h is unchanged

For now, let’s assume excitons are the information carrier

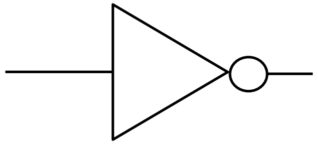
Logical 0 and 1 States in Momentum Space



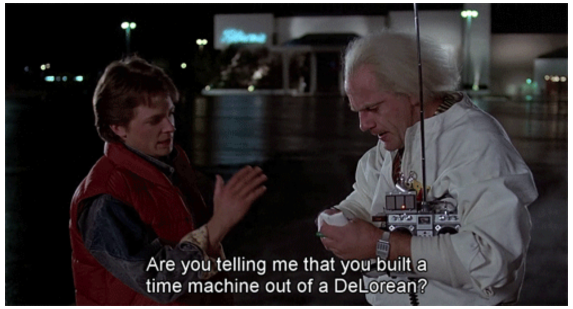
Can initialize and readout $|0\rangle$ and $|1\rangle$ states

	Parameter	Logical "0"	Logical "1"
CMOS	Voltage	Low	High
Valleytronic	Particle crystal momentum	K	-K

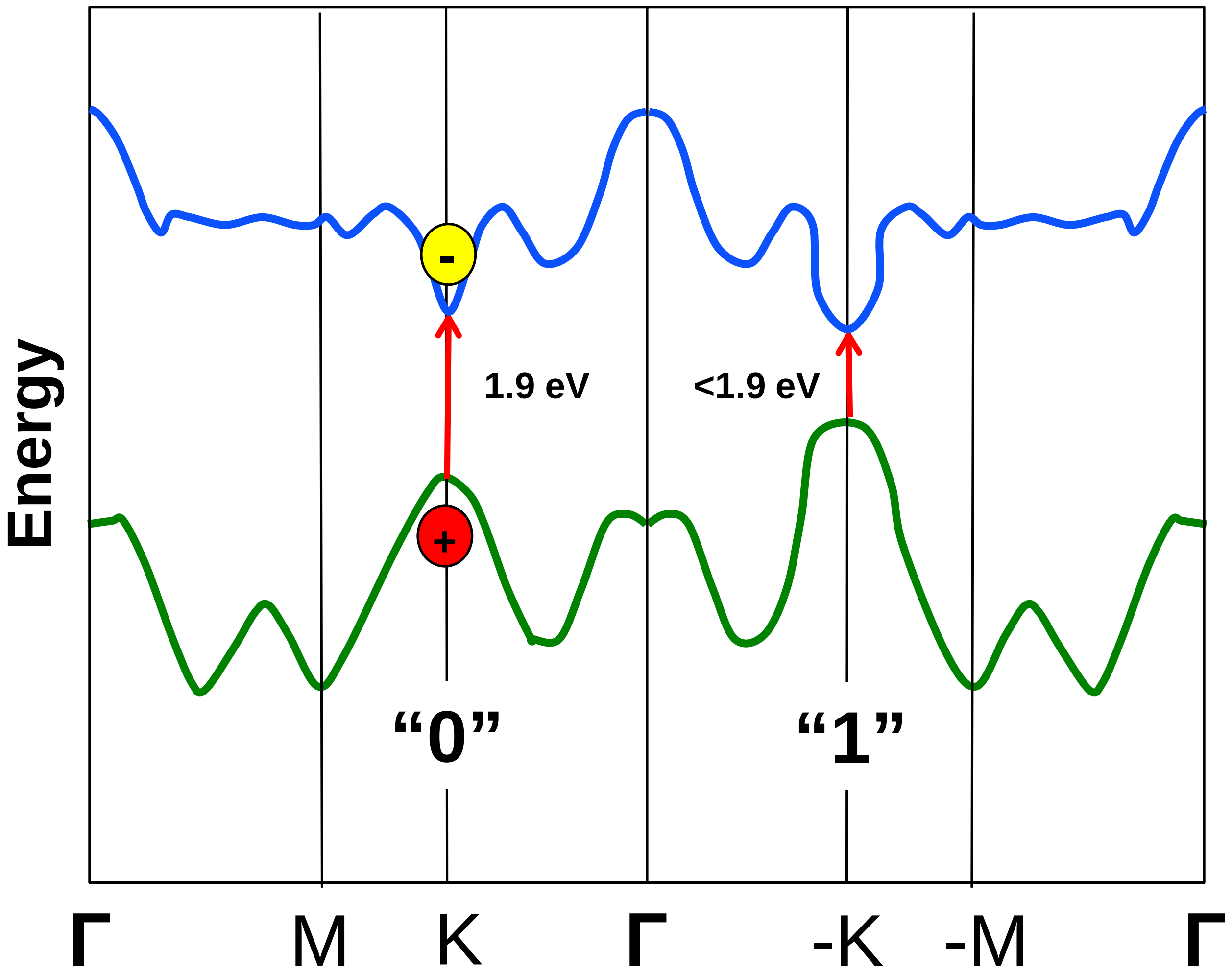
But … how do we switch a $|0\rangle$ to a $|1\rangle$?



$$|K\rangle \xrightarrow{T:\ t \longrightarrow -t} |-K\rangle$$



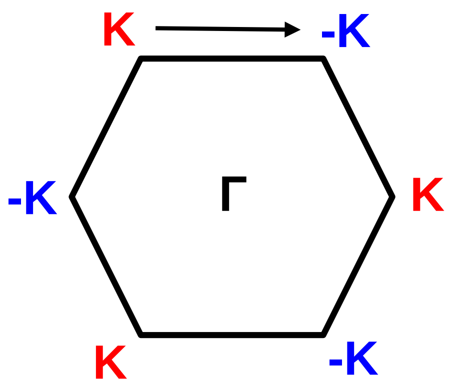
Can We Do It By Breaking Valley Degeneracy?

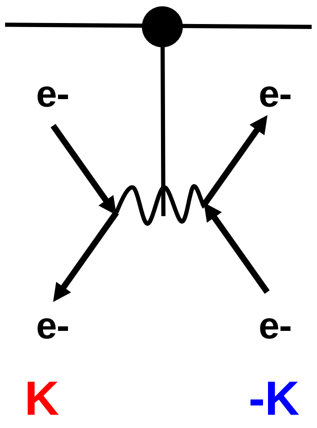


Shift energy of K valley vs -K valley via:

- **Optical Stark Effect** [Sie, Nature Materials, 2015]
- **Zeeman Effect** [MacNeil, PRL, 2015]
- **Magnetic Proximity Effect** [Zhong, Sci Adv, 2017]

Well … a $|K\rangle$ state probably will not evolve to a $|-K\rangle$ state since they are momentum protected

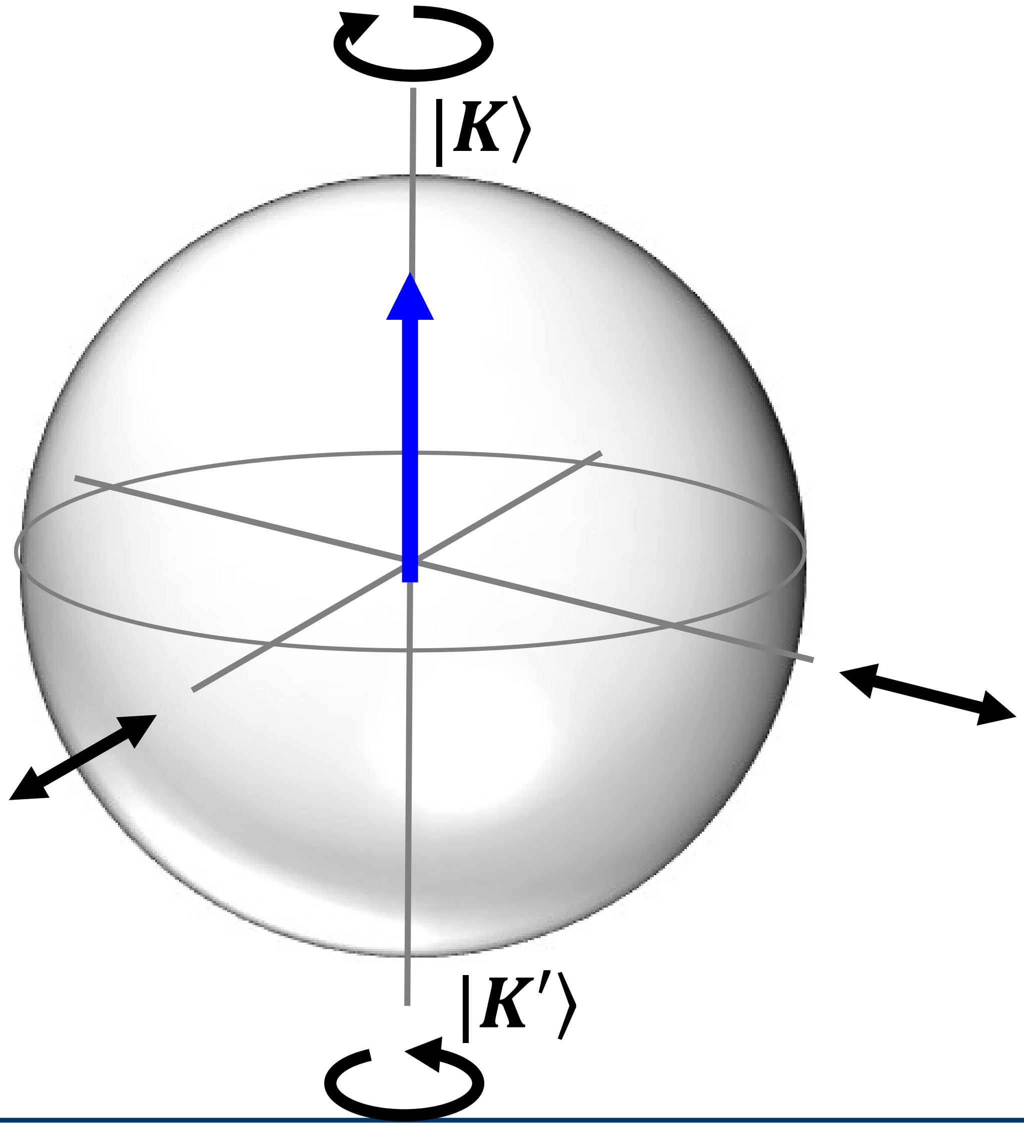


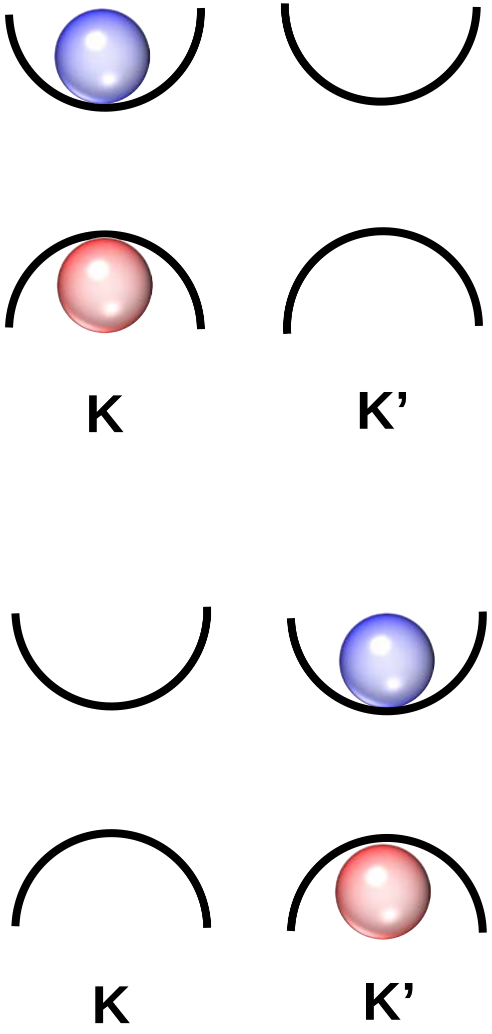


Deterministic Switching from 0 to 1: $|K\rangle$ to $|K'\rangle$

$$|R\rangle = \frac{1}{\sqrt{2}}(|x\rangle + i|y\rangle)$$

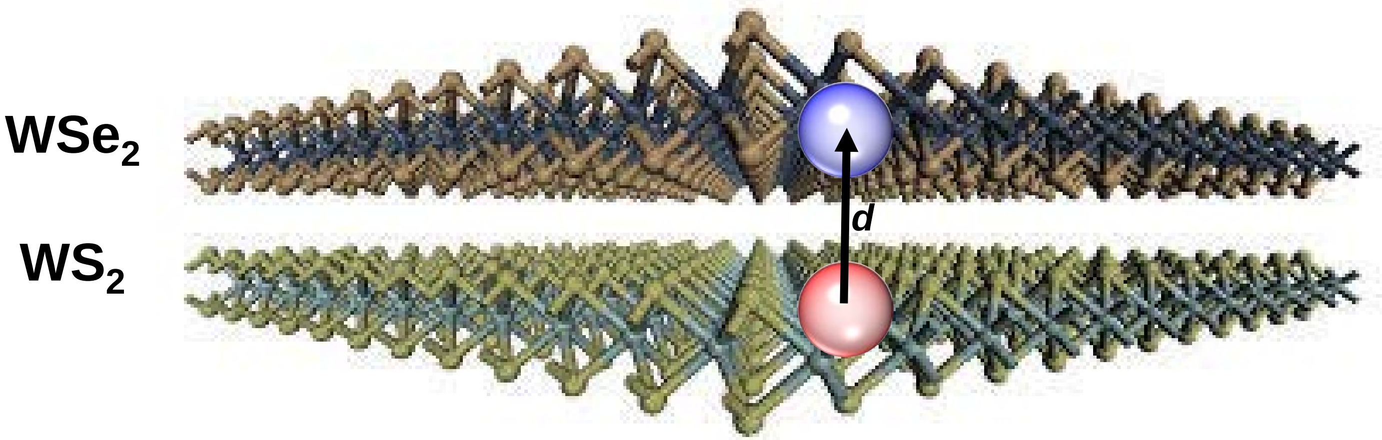
Hard problem #1: figure out a way to deterministically flip an exciton between $|K\rangle$ and $|-K\rangle$ states



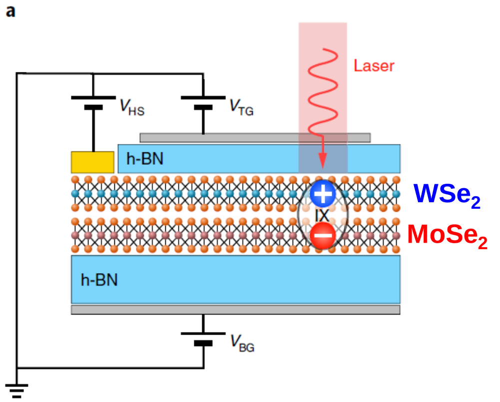


$$|L\rangle = \frac{1}{\sqrt{2}}(|x\rangle - i|y\rangle)$$

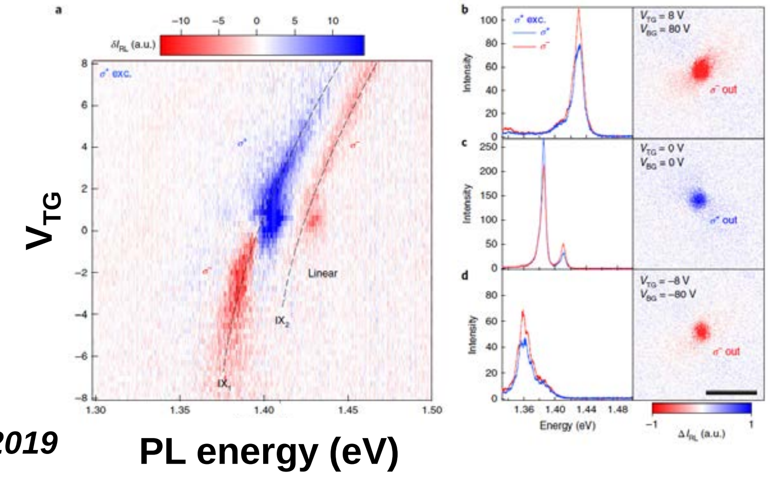
Perhaps Using Spatially Indirect Excitons



- Bilayer of two different TMDs with Type II band alignment
- Electron resides in one layer, hole resides in other layer
- Spatial separation forces an out-of-plane static dipole
- Maybe flip dipole (and valley) electrostatically?

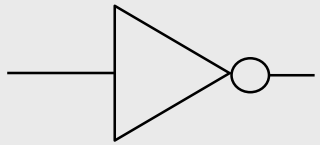


Ciarrocchi et al, Nature Photonics, Feb 2019



Need to increase contrast and reduce voltage

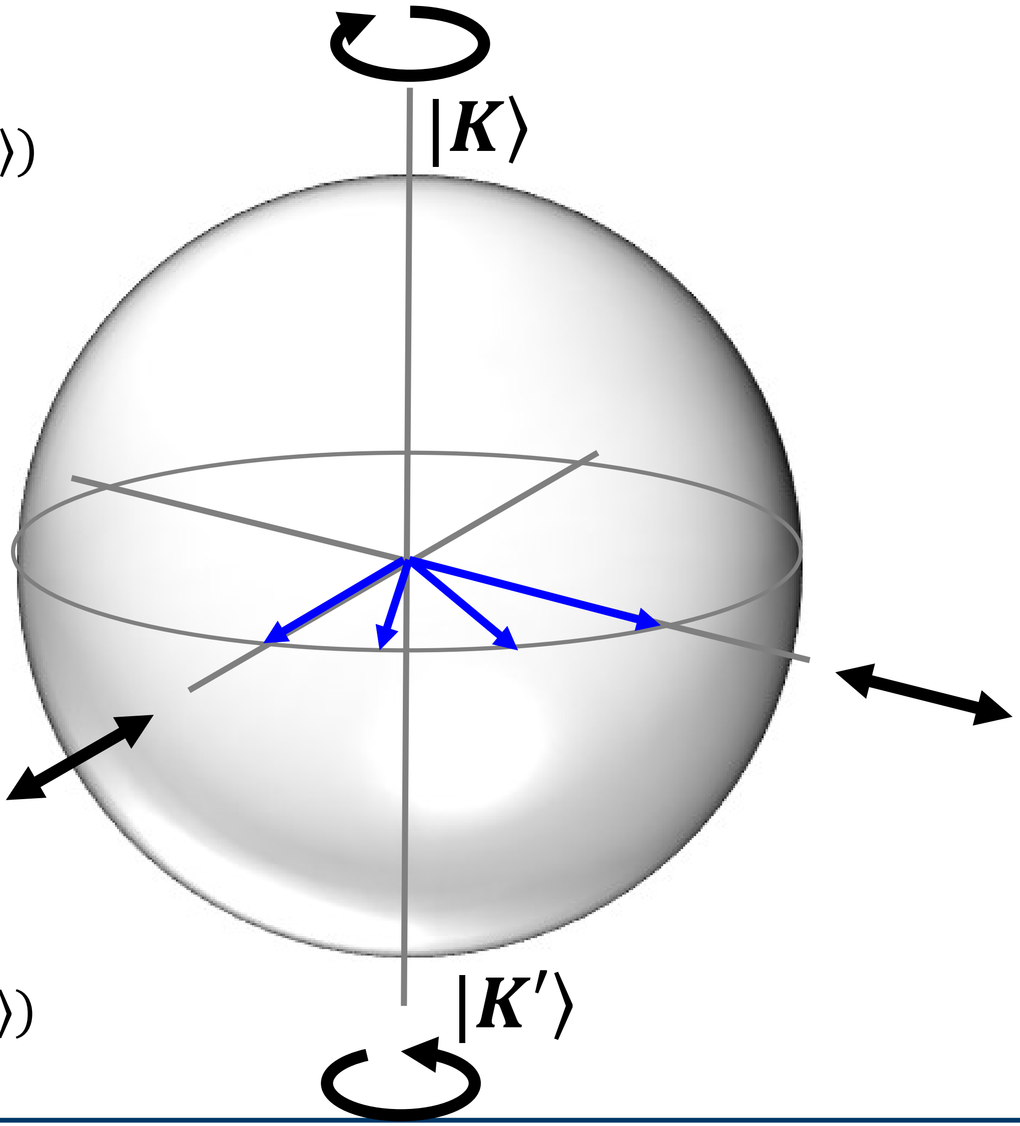
Possible route to an



Deterministic Switching from 0 to 1: $|X\rangle$ to $|Y\rangle$

$$|X\rangle = \frac{1}{\sqrt{2}}(|x\rangle + i|y\rangle) + \frac{1}{\sqrt{2}}(|x\rangle - i|y\rangle)$$

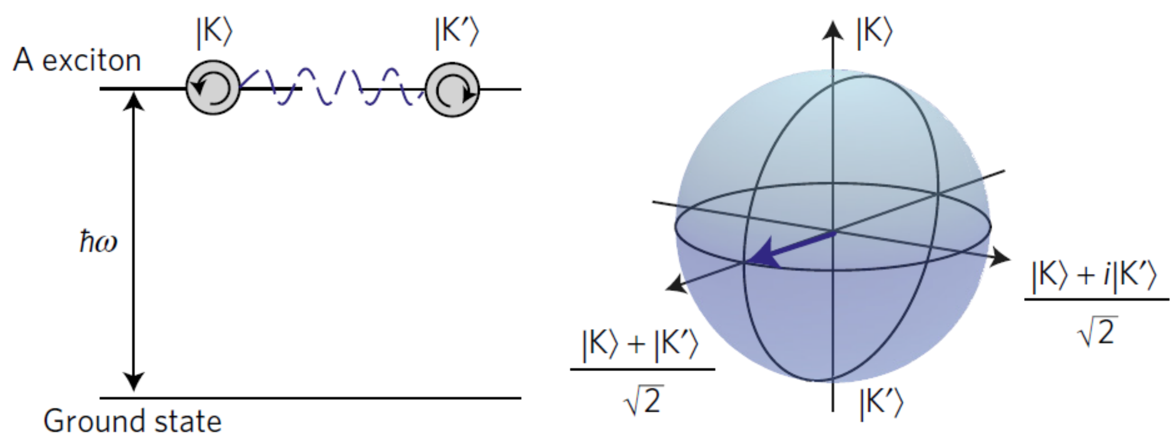
$$E_K \geq E_{K'}$$



$$|Y\rangle = \frac{1}{\sqrt{2}}(|x\rangle + i|y\rangle) - \frac{1}{\sqrt{2}}(|x\rangle - i|y\rangle)$$

Deterministic Switching from 0 to 1: $|X\rangle$ to $|Y\rangle$

a *Ye, Sun, Heinz, Nature Physics, 2016*



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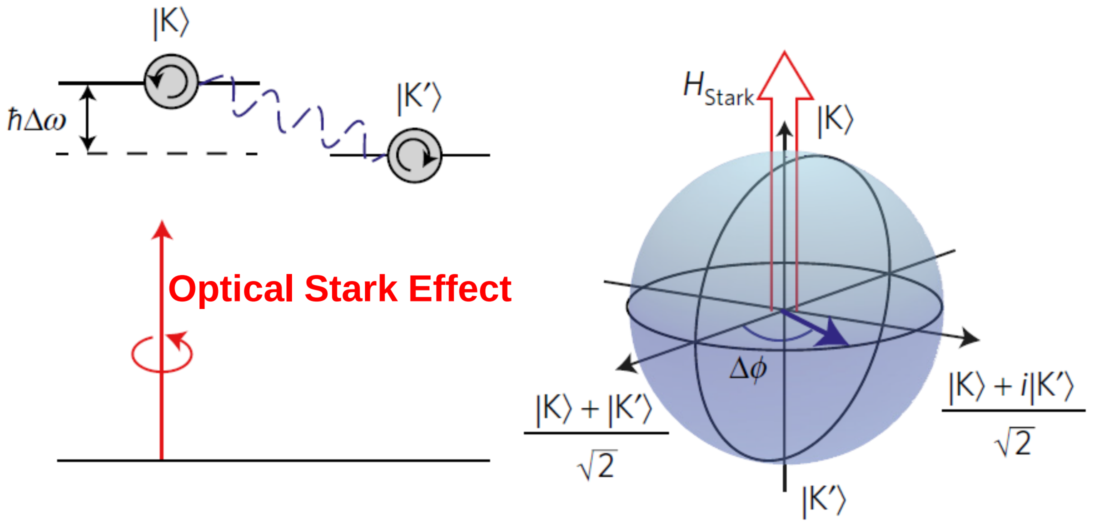
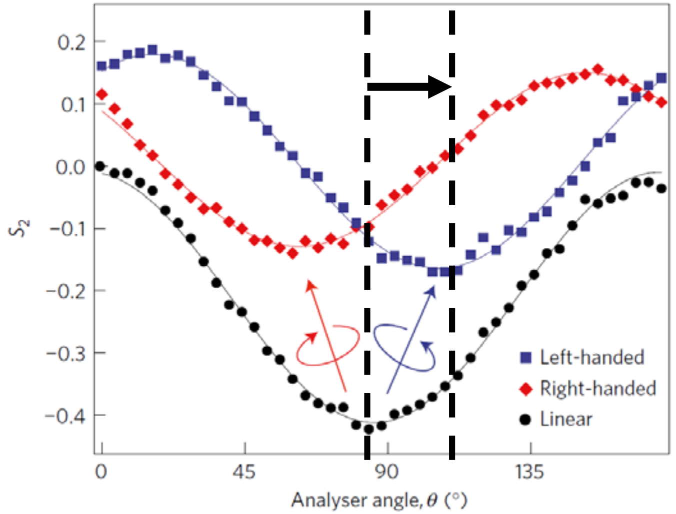
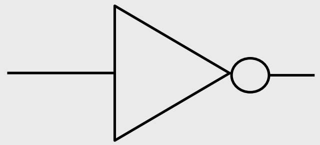




$$S_x = \frac{S_{xo}}{1 + \left(\Omega T^*_{S2}\right)^2} \qquad S_y = \frac{\Omega T^*_{S2} S_{xo}}{1 + \left(\Omega T^*_{S2}\right)^2} \qquad \hbar\Omega = g\mu_B B$$

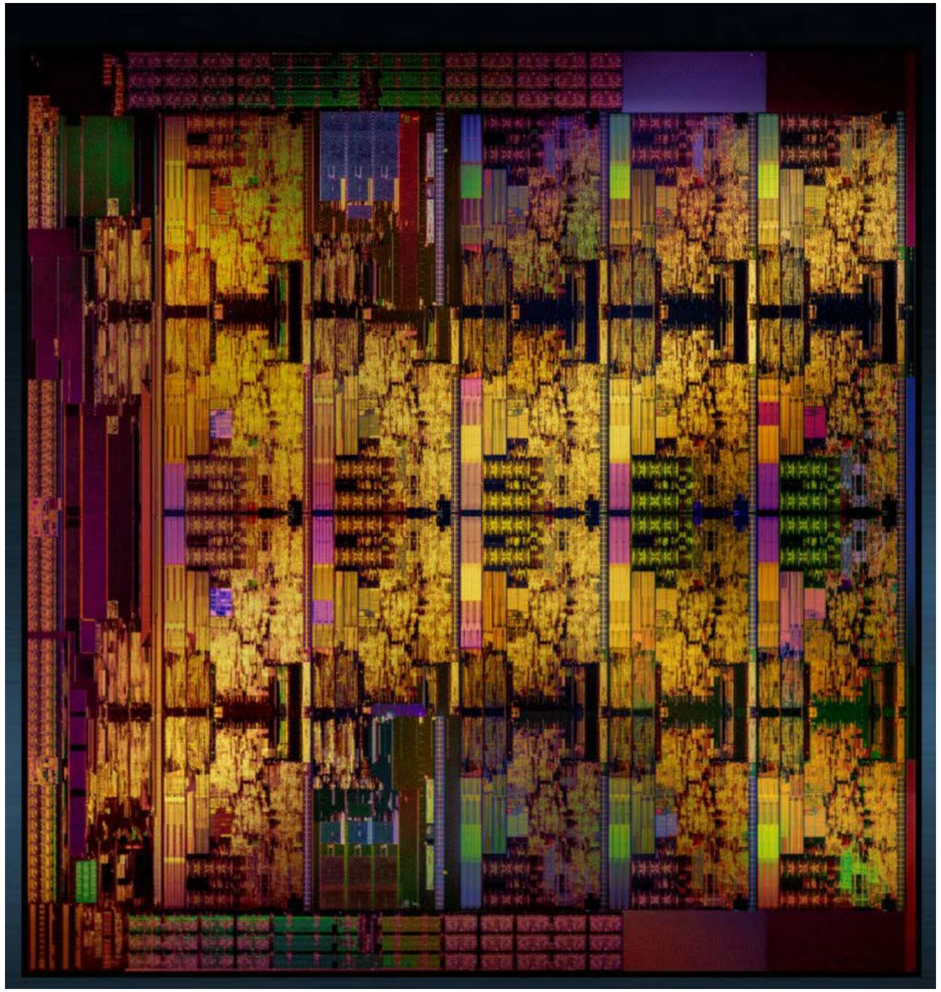
Precession of valley polarization by 40º demonstrated, limited by valley coherence time and Stark field

Possible route to an



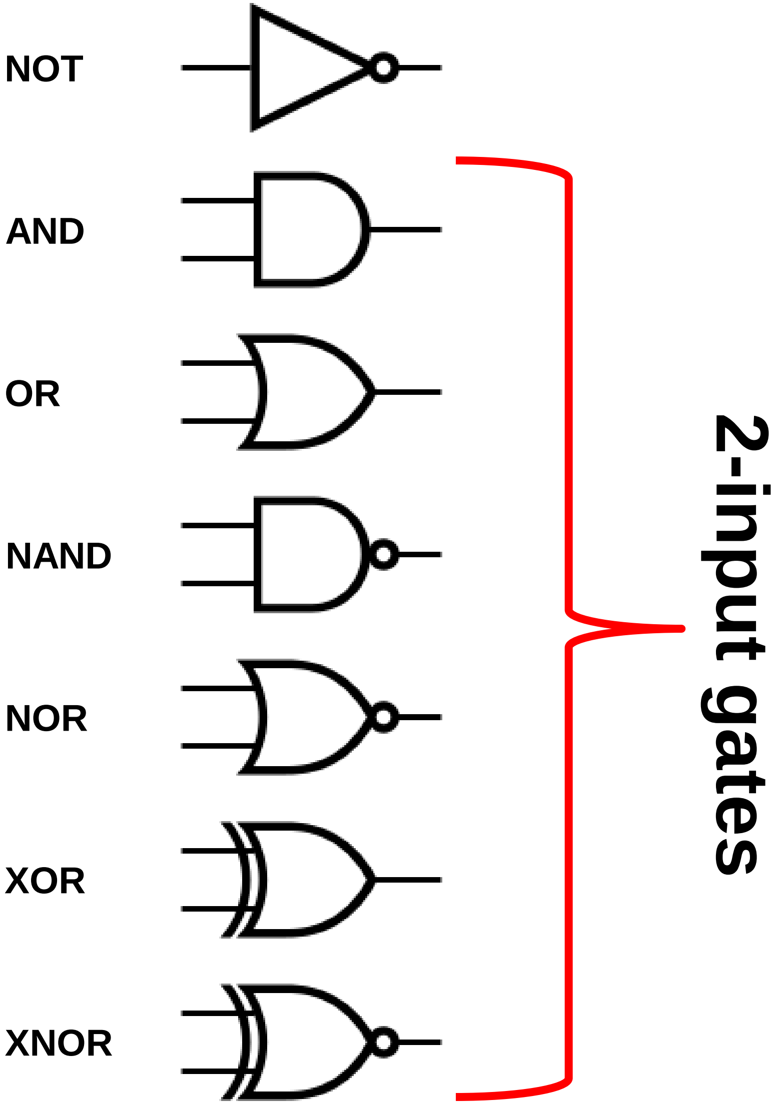
That’s nice, but did anyone notice the 800 pound Gorilla?

- Intel Core i9-7980XE
- 18 CPU cores
- 14nm++ process
- Approx. 8 billion transistors

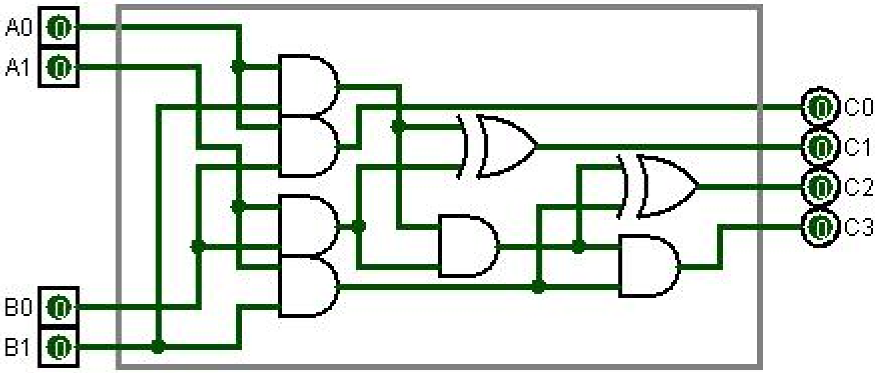


We’re going to need more than an inverter ...

Need Complete Set of Logic Gates



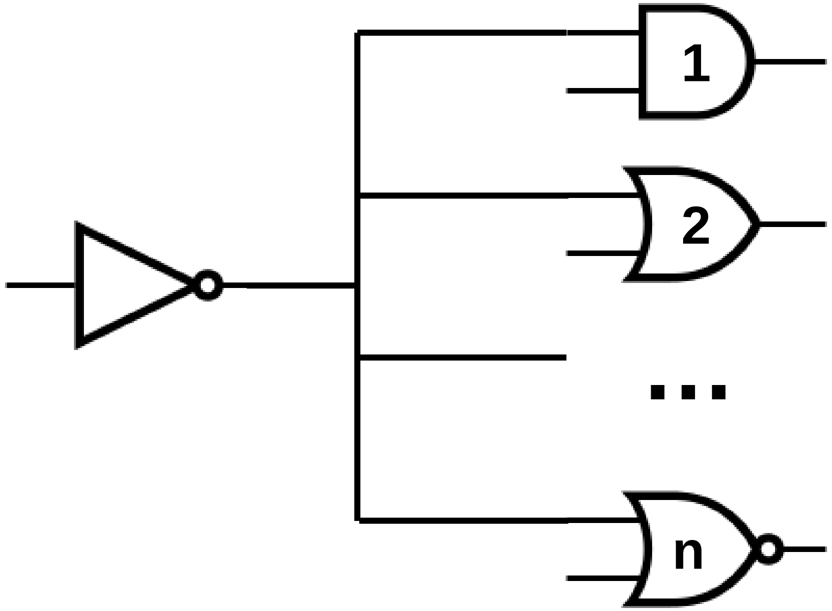
2 bit multiplier



- **Any non-trivial circuit requires <u>concatenation</u>**
- **All inputs and outputs <u>must be in the same domain</u>: excitons-in → excitons-out**
- **Could have an ancillary control line in a different domain**

Hard problem #2: develop a viable set of 2-input exciton logic gates

Concatenation Implies Fan-Out and Gain



- **Must have some way to vary the drive strength of valley gates**
- **For silicon CMOS this is easy: drive current is proportional to transistor width**
- **One gate wide transistor can provide the input to many smaller gates**

Hard problem #3: Demonstrate a device that supports exciton fan out and gain

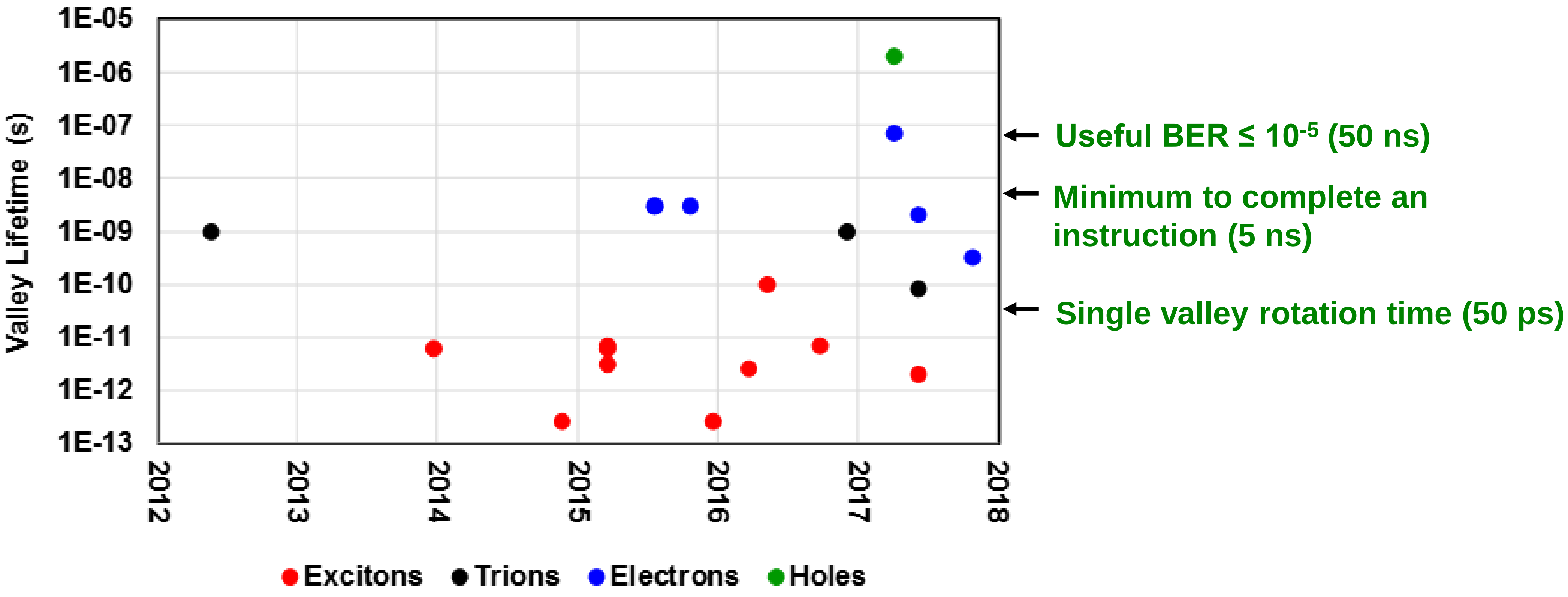
Valley Lifetime

- Valley information has a rather short lifetime
- How long does the valley lifetime have to be?
- In a classic RISC architecture there are five stages

- Assume:
  - simple non-pipelined CPU
  - simple 1-cycle execution stage
  - valley information transport velocity ≈ CMOS info transport velocity*
- Need ~ 5 ns to complete an instruction

* Requires gate speed o(100 ps)

Measured Valley Lifetime



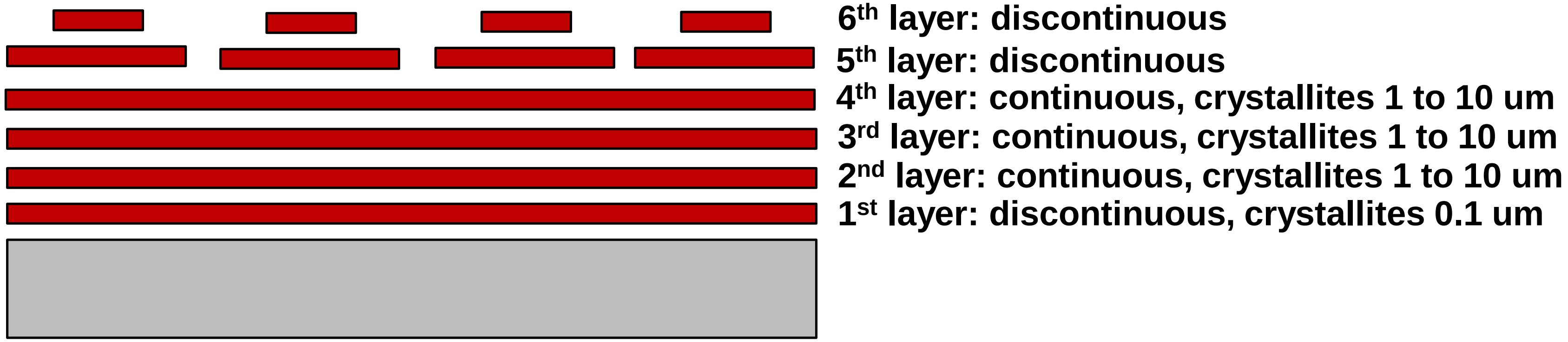
Valley lifetimes approaching that needed for practical computation have been measured for electrons and holes, but not for excitons. Need to improve material quality.

Valleytronic Quality Material

Valleytronic Quality Material

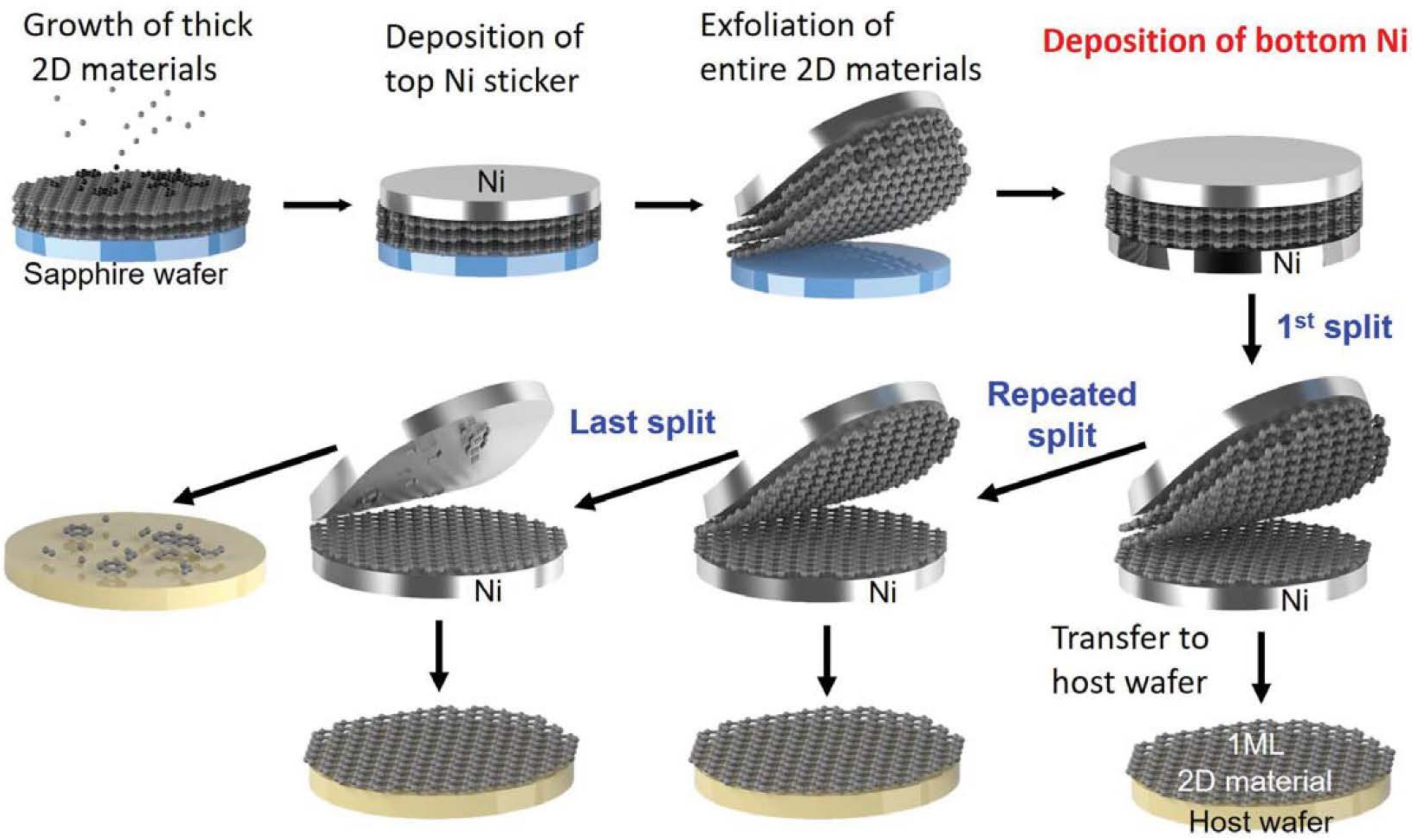
- Grown material (e.g., CVD, MBE, ALD) is the only practical option
- So far, monocrystalline, monolayer TMD growth has not been demonstrated
  - Growth process is not self limiting
- Many reports of “wafer scale” growth but these are polycrystalline, multilayer, or both

Typical:



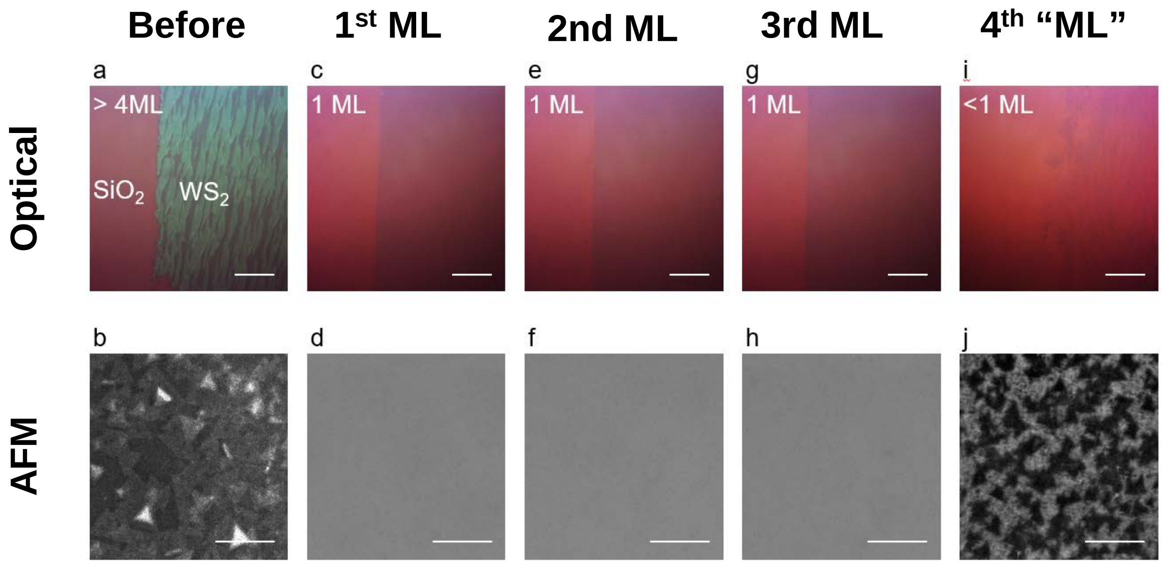
How do we get decent wafer-scale monolayer material?

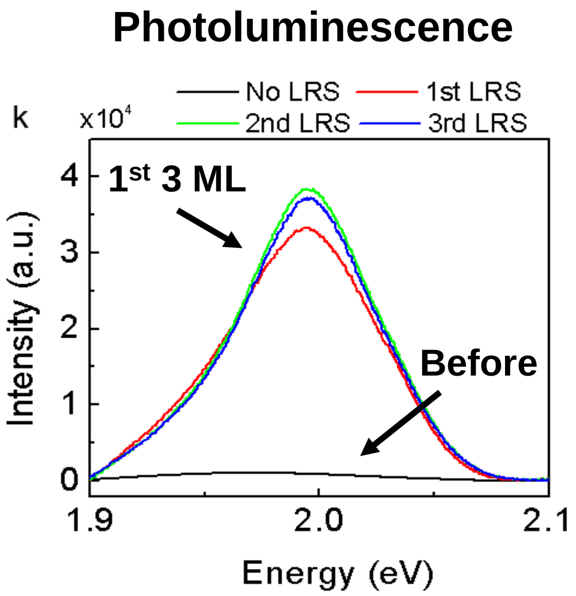
Valleytronic Quality Material

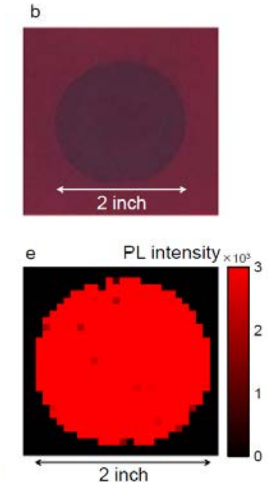


Shim et al, Science, 2018

Successful Layer Resolved Splitting







Isolation of wafer scale monolayer 2D material is an important advancement

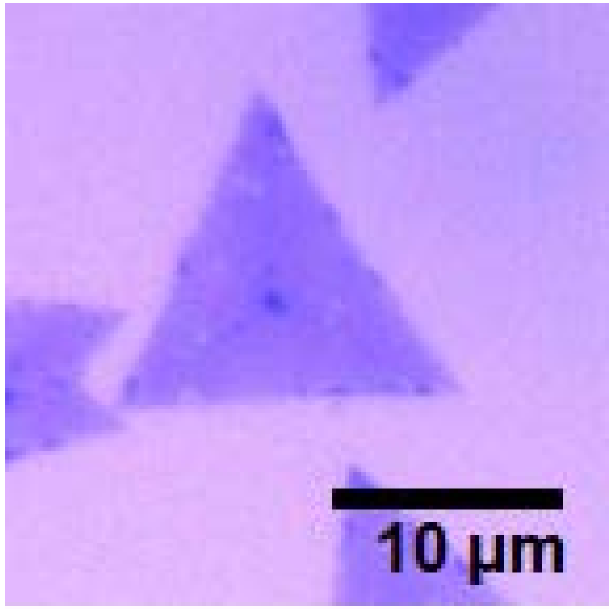
But, the material is still polycrystalline …

When Reality Sets In

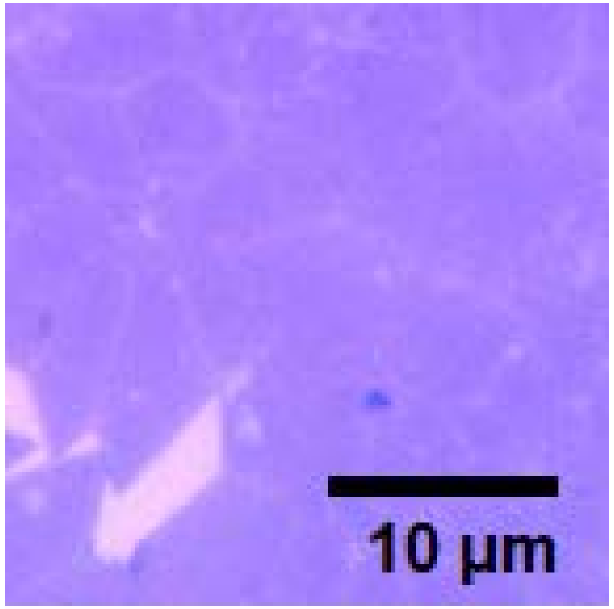
A Look at Real TMD Materials

CVD Grown MoS_2

<u>Single crystals</u>: 1 to 100 µm



<u>Polycrystalline monolayers</u>: µm's to cm's

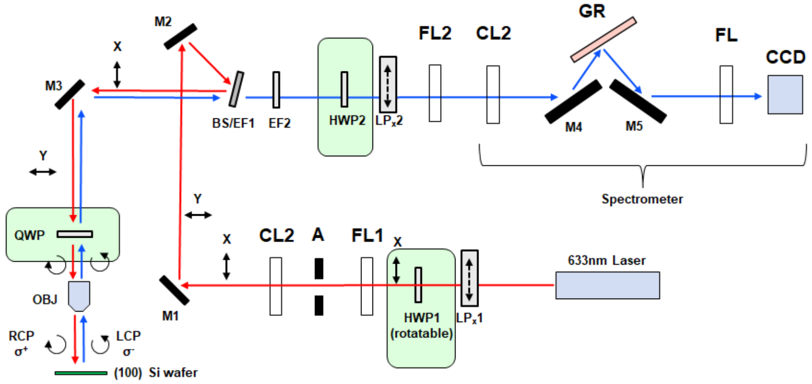


- **Are Valleytronic properties preserved in polycrystalline monolayers?**
- **Or do we need to grow cm-scale single crystals for integrated device fabrication?**

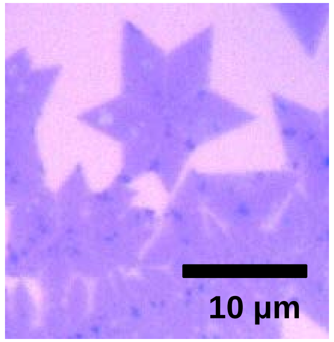
Measure valley photoluminescence polarization across various crystal morphologies

Raman-corrected Photoluminescence Imaging

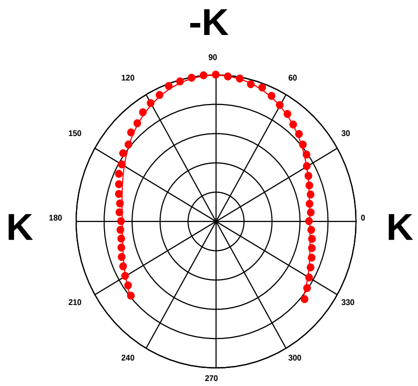
Simultaneous polarized Raman and PL



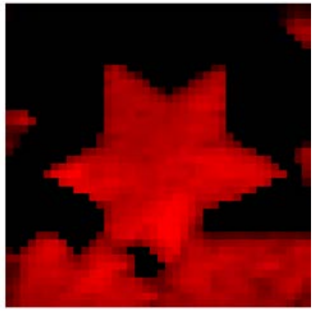
Optical



PL vectors at many incidence polarizations



Valley Polarization Imaging

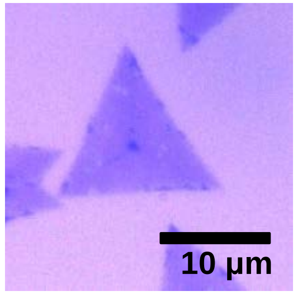


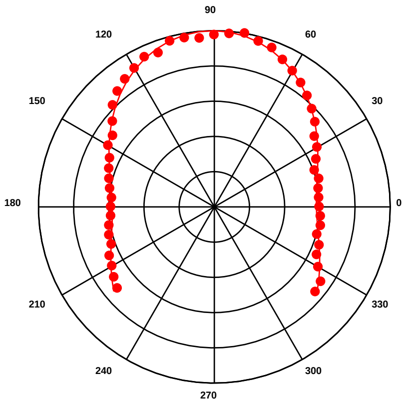
Allows precise, artifact-free measurement of valley initialization

Effect of Morphology on Valley Polarization

Temperature = 4 K

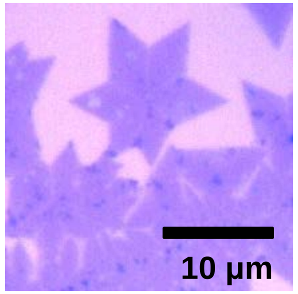
Triangle

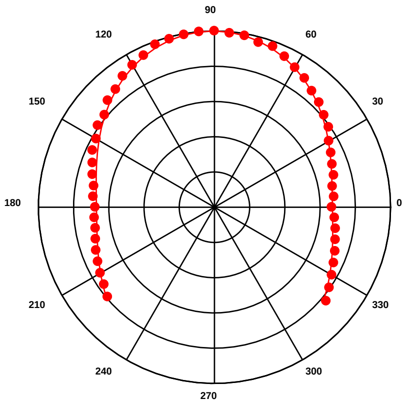




42% polarization

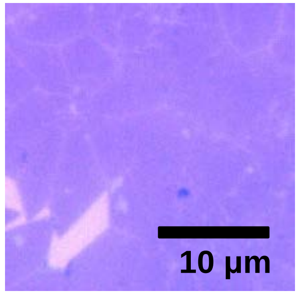
Star

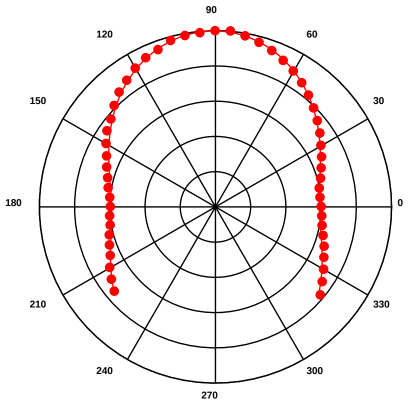




32% polarization

Merged





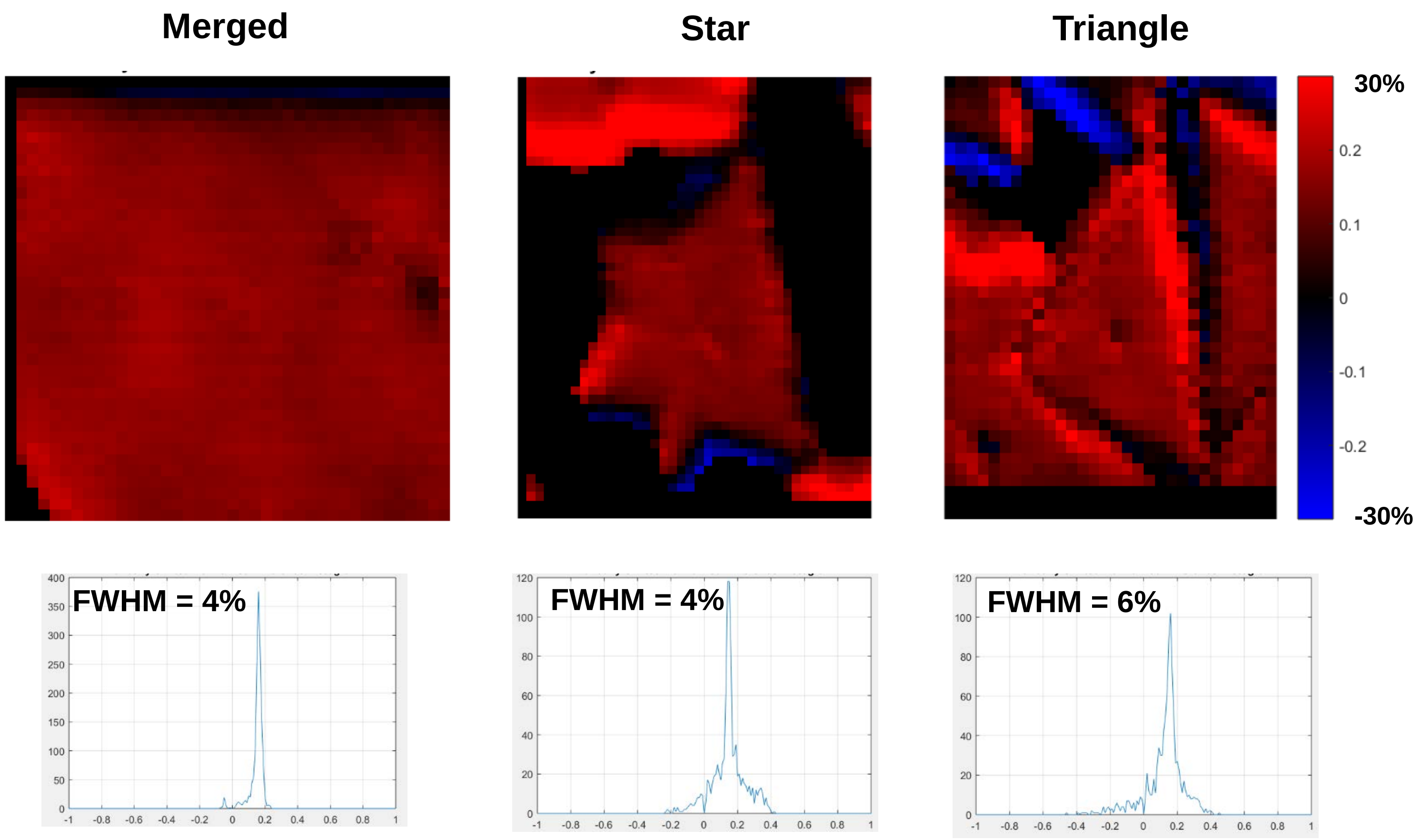
41% polarization

Domain boundaries and polycrystallinity does not strongly degrade valley polarization

Note: spot size 1µm << domain size

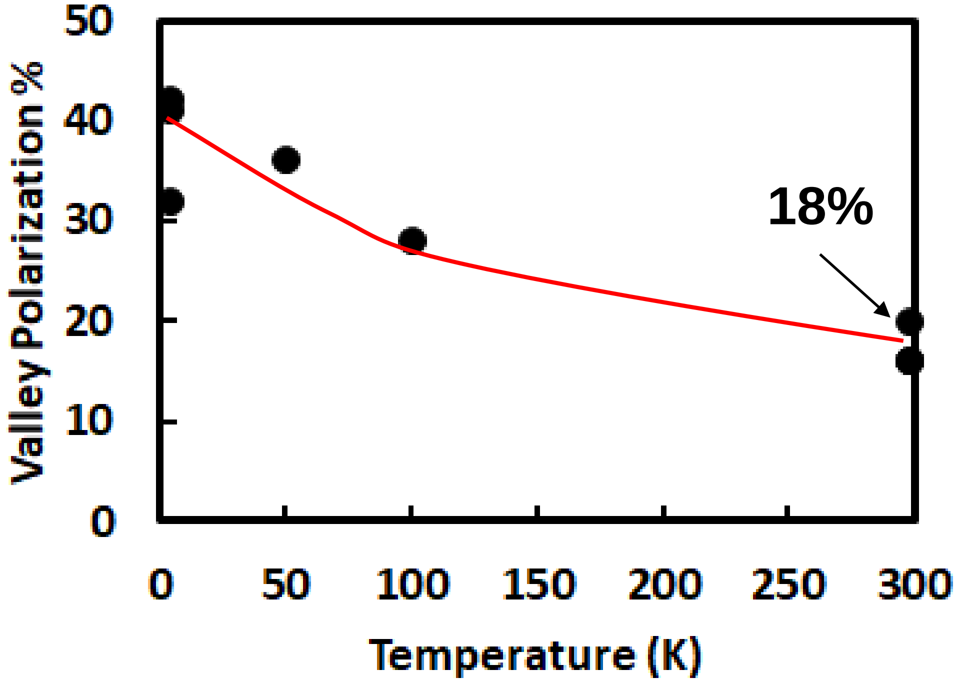
Valley Polarization Mapping

Temperature = 4 K



Remarkably, valley polarization uniformity is comparable for polycrystalline and single crystal domains

What about at Room Temperature?



Need significant improvement in state initialization

Towards Efficient State Initialization

Steady State PL polarization:

$$P_{circ} = \frac{P_o}{1 + 2\frac{\tau_{exc}}{\tau_v}}$$

Exciton lifetime (τ_{exc})

Valley lifetime (τ_v)

Kioseoglou et al., Appl Phys Lett, 2012.

- **Can get very high polarization if τ_{exc} is short**
- **But for computation need long τ_{exc} and $\tau_v >> \tau_{exc}$**

	Decreased by	Increased By
Exciton Lifetime	**Strong binding energy Small Bohr radius Recombination centers**	**Strain Localization**
Valley Lifetime	**Exchange interaction Phonons Magnetic scattering centers**	**SOC Substrate isolation**

A Tale of Two Valleys

It was the best of times, it was the worst of times, it was the age of wisdom, it was the age of foolishness, it was the epoch of belief, it was the epoch of incredulity, it was the season of Light, it was the season of Darkness, it was the spring of hope, it was the winter of despair …

- **Valleytronics offers a new degree of freedom for information processing**
- **For classical computing, the key bottleneck for new logic devices is switching energy**
  - **Any logic device based on diffusion/drift of charge will be no better (or only marginally better) than conventional silicon CMOS**
- **Computation based on valley-polarized excitons is plausible but there are several hard problems to be solved**
  - **figure out a way to deterministically flip an exciton between $|K\rangle$ and $|-K\rangle$ states**
  - **develop a viable set of 2-input exciton logic gates**
  - **demonstrate exciton fan out and gain**
- **Alternatively, it might be easier to develop a valley tunnel FET**